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10/757,750	01/14/2004	Christopher A. Menkus	08211/0200349-US0/P05782	4265

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EXAMINER	
NGUYEN, LINH V	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,750	MENKUS, CHRISTOPHER A.	
	Examiner	Art Unit	
	Linh V. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26-34,40 and 42-51* is/are rejected.

7)☒ Claim(s) *35-39 and 41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to applicant's amendment filed on 11/15/05. Claims 1 – 25 have been canceled. New claims 26 – 51 have been added. Claims 26 – 51 are pending on this application.

Response to Arguments

2. Applicant's arguments filed under remarks have been fully considered but they are not persuasive.

With respect to claims 26, 40, 43, 45, and 51, under remarks, on page 16, applicant argued, "the coarse offset calibration 304 of Lee does not calibrated the coarse channel (coarse ADC 203 of Fig. 2 of Wang). Rather, coarse offset calibration circuit 304 of Lee provides coarse offset calibration for analog input signal of the ADC". Examiner respectful disagrees from the following:

Claimed invention is claiming for folding analog to digital converter having a coarse channel calibration circuit for coarse. While Wang et al. (Fig. 1) teaches a folding analog-to-digital converter having a coarse channel for analog-to-digital converter, but Wang does not disclose a coarse channel calibration.

Fig. 3 of Lee disclosing an analog-to-digital conversion circuit (350) having a coarse offset calibration (304) which generating offset signal (326) to calibrating for the coarse signal of Analog to Digital conversion circuit (350). Therefore, Lee clearly suggested a coarse channel calibration for coarse signal of analog-to-digital converter.

Accordingly, the combination of Lee into the coarse analog-to-digital converter 203 of Wang is proper.

Per discussed above, the reference from previous office action is applying in this office action.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 26, 40, 43, 45 – 48, and 50 – 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. U.S. Patent No. 6,535,156 in view of Lee et al.

Regarding claim 26, Fig. 1 of Wang et al. discloses an analog-to-digital conversion converter comprising: a fine channel circuit (202) that includes folding stages (Col. 2 lines 8 – 13); a coarse channel circuit (203) with adjustment circuit (321). However, Wang et al. does not disclose a coarse channel calibration circuit.

Fig. 3 of Lee et al. discloses an analog-to-digital converter circuit (305) comprising: coarse channel calibration circuit (304) and fine channel adjustment circuit (308).

Wang et al., Lee et al. are common subject matter for analog to digital converter. Therefore it would have been obvious to one having ordinary skill in the art at the time

the invention was made to incorporated the coarse calibration of Lee et al. into the coarse channel of Wang et al. for the purpose of providing adjusting offset of input signal and adjust signal gain such that the full dynamic range of system is utilized (Lee et al., Col. 3 lines 14 – 28).

Regarding claim 40, the claim incorporated the same subject matter as of claim 26 and rejected along the same rationale.

Regarding claim 43, Fig. 1 (203) coarse channel of Wang et al. combined with Fig. 3 coarse channel calibration (304) for coarse channel analog to digital converter (306) as applied to claim 26 above disclosed every aspect of applicant claimed invention. Therefore, claim 43 is rejected along the same rationale as of claim 26.

Regarding claim 45, the claim incorporated the same subject matter as of claim 26, and rejected along the same rationale.

Regarding claim 46, Wang/Lee et al as applied to claim 26 above, Wang (Fig. 1) further disclose the fine channel circuit (201) is arranged to perform a fine analog –to-digital conversion of an input signal (206); and wherein the coarse channel circuit (201) is arranged to perform analog-to-digital conversion of the input signal (206) in parallel with fine analog to digital converter (201).

Regarding claim 47, the claim incorporated the same subject matter as of claim 26 and rejected along the same rationale.

Regarding claim 48, Wang (Fig. 1) further discloses the coarse channel circuit (203) includes an amplifier array.

Regarding claim 50, the claim incorporated the same subject matter as of claim 46 and rejected along the same rationale.

Regarding claim 51, the claim incorporated the same subject matter as of claim 40, and rejected along the same rationale.

5. Claims 27 – 34, 42, 44, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al and Lee et al. as applied to claim 26 above, and further view of Chen et al. U.S. Patent No. 6,628,216.

Regarding claim 27, Wang/Lee et al. as applied to claim 26 above does not discloses a control circuit that is configured to provide a select signal; and a voltage reference circuit that is configured to provide a voltage reference signal that corresponds to the select signal wherein the coarse channel circuit is configured to receive the voltage reference signal.

Fig. 8 of Chen et al. discloses an analog to digital converter comprising: a control circuit (807) that is configured to provide a select signal (801); and a voltage reference circuit (139) that is configured to provide a voltage reference signal (output of 13) that corresponds to the select signal (output of 807), wherein the coarse channel circuit (805; See Col. 18 lines 18 - 21) is configured to receive the voltage reference signal.

Wang/Lee et al. and Chen et al. are common subject matter for analog to digital converter. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the control circuit of Chen into the

Wang/Lee converter for the purpose of providing the controlling of reference voltages, thereby providing accuracy for analog-to-digital converter.

Regarding claim 28, Wang/Lee et al. as applied to claim 26 above does not discloses wherein the coarse channel circuit is configured to provide an output signal in response to a voltage reference signal and wherein the coarse channel calibration circuit is configured to: receive a feedback signal from the coarse channel circuit, and provide an adjustment signal to the coarse channel circuit in response to the feedback signal.

Chen et al. as applied to claim 27 above, further discloses (Fig. 8 of Chen et al.) wherein the coarse channel circuit (805) is configured to provide an output signal (output of 805) in response to a voltage reference signal (139), and wherein the coarse channel calibration circuit (805) is configured to: receive a feedback signal (Output of output of 805) from the coarse channel circuit (Fig. 8), and provide an adjustment signal (output of 811) to the coarse channel circuit in response to the feedback signal (Col. 4 line 64 – Col. 5 line 9).

Wang/Lee et al. and Chen et al. are common subject matter for analog to digital converter. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate feedback of Chen into the Wang/Lee converter for the purpose of providing feedback for controlling the output of analog to digital converter.

Regarding claim 29, Wang/Lee et al. as applied to claim 26 above does not discloses wherein the coarse channel circuit comprises an amplifier array and a

comparator array wherein at least one the amplifier array or comparator array is configured to received an adjustment signal.

Chen et al. as applied to claim 27 above, further discloses wherein the coarse channel circuit (Chen et al. Fig. 6) comprises an amplifier array (PA) and a comparator array (C0...C13) wherein at least one the amplifier array or comparator array is configured to received an adjustment signal (Chen et al. Fig. 1[134, 135]).

Wang/Lee et al. and Chen et al. are common subject matter for analog to digital converter. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the comparator of Chen into the Wang/Lee converter for the purpose of comparing the input signal with reference voltages the generating digital output signal.

Regarding claim 30, the claim incorporated similar subject matter feedback signal as of claim 3, and rejected along the same rationale.

Regarding claim 31, Wang/Lee as applied to claim 26 above, does not disclose a coarse channel calibration circuit; wherein the coarse channel calibration circuit includes a counter circuit coupled to the adjustment circuit (312).

Chen et al. as applied to claim 27 above, Chen et al. further disclosing wherein the coarse channel calibration circuit (Fig. 8) includes a counter circuit (809) and a parameter adjustment circuit (811) that is couple to the counter circuit (809).

Wang/Lee et al. and Chen et al. are common subject matter for analog to digital converter. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the counter of calibration circuit

taught by Chen et al. into the calibration of Wang/Lee for the purpose of providing a predetermined internal to generated the sum value of the output stream bits (Chen et al.; Col. 18 lines 18 – 24).

Regarding claim 32, Wang/Lee/Chen as applied to claim 31 above, Chen (Fig. 8) further discloses wherein the adjustment circuit (302) includes a DAC (312) to provide a converted signal (output of 312) to the coarse channel signal.

Regarding claim 33, Wang, Lee and Chen et al. as applied to claim 1 above, and (Fig. 8) of Chen et al. further discloses a feedback signal (BitS), the counter circuit (809) received the feedback signal (BitS), the parameter adjustment circuit (811) receive the count signal (SUM) and adjustment parameter (output of 811) response to the count signal (SUM).

Regarding claim 34, Chen et al. as applied to claim 8 above, further discloses wherein the parameter comprises one single-ended current or differential current (Chen et al., Col. 26 lines 10 – 13).

Regarding claim 42, Wang/Lee as applied to claim 40 above, does not disclose wherein the coarse channel calibration circuit includes a counter circuit that is configured to provide a count signal in response to the timing signal and the output signal coupled, and parameter adjustment circuit that is configured to adjust the parameter in response to the count signal

Chen et al. as applied to claim 27 above, further disclosing wherein the coarse channel calibration circuit (Fig. 8) includes a counter circuit (809) that is configured to provide a count signal (Sum) in response to the timing signal (CLK) and the output

(BITS) and a parameter adjustment circuit (811) that is configured to adjust the parameter in response to the count signal (SUM).

Wang/Lee et al. and Chen et al. are common subject matter for analog to digital converter. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the counter of calibration circuit taught by Chen et al. into the calibration of Wang/Lee for the purpose of providing a predetermined internal to generated the sum value of the output stream bits (Chen et al.; Col. 18 lines 18 – 24) for generating the adjustment signal thereby improve the output of the converter.

Regarding claim 44, Wang/Lee as applied to claim 43 above, does not disclose wherein receiving a signal from the coarse channel circuit after providing the reference voltage; and adjusting a count in response to the signal, wherein the parameter is adjusted according to the count.

Chen et al. as applied to claim 27 above, further disclosing wherein the coarse channel calibration circuit (Fig. 8) includes receiving a signal from the coarse channel circuit (BITS) after providing the reference voltage (139); and adjusting a count (809) in response to the signal (BITS), wherein the parameter is adjusted (811) according to the count (SUM).

Wang/Lee et al. and Chen et al. are common subject matter for analog to digital converter. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the counter of calibration circuit taught by Chen et al. into the calibration of Wang/Lee for the purpose of providing a

predetermined internal to generated the sum value of the output stream bits (Chen et al.; Col. 18 lines 18 – 24) for generating the adjustment signal thereby improve the output of the converter.

Regarding claim 49, the claim incorporated the same subject matter as of claim 28, and rejected along the same rationale.

Allowable Subject Matter

5. Claims 35 – 39, and 41 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 35, prior arts fail to teach a folding Analog-to-Digital converter comprising a counter circuit is configured to, if latched: increment a count value that is associated with the count signal if the comparator output response to a first level, and decrement the count value if the comparator output response to a second logic level.

With respect to claim 38, prior art fails to teach wherein the parameter adjustment circuit includes a first digital-to-analog converter circuit that is configured to convert the count signal into a first analog signal; and a second digital-to-analog converter circuit that is configured to convert an inverted count signal into a second analog signal.

With respect to claim 39, prior art fails to teach a control circuit providing a selecting signal, and provide a timing signal at a predetermined amount of time after providing the select signal, wherein the coarse channel calibration circuit is configured to latch the output signal in response to the timing signal.

With respect to claim 41, prior art fails to teach assert a timing signal for latching the coarse channel calibration circuit at a predetermined amount of time after a change of select signal.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

6. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Rexford Barnie can be reached at (571) 272-7492. The fax phone numbers for the organization where this application or proceeding is assigned are (571-273-8300) for regular communications and (571-273-8300) for After Final communications.

01/17/06

Linh Van Nguyen 

Art Unit 2819